Claims:

What we claim are:

1. A wafer level flip chip package process for manufacturing flip chip assemblies for semiconductor chips or devices, comprising the process steps of:
   - preparing a substrate wafer wherein said substrate wafer is precisely lapped and polished to minimize the total thickness variation;
   - preparing a submount wafer wherein said submount wafer is precisely lapped and polished to minimize the total thickness variation;
   - growing an epitaxial layer onto said substrate wafer to form an epitaxial wafer of semiconductor chips or devices; wherein said epitaxial layer comprising first confinement layer , active layer, and second confinement layer stacked on said substrate wafer; and wherein the thickness of said first confinement layer is predetermined to compensate the combination of the total thickness variations of said substrate and said submount wafers;
   - disposing reflective and Ohmic contact layers on said second confinement layer;
   - disposing a first and a second solderable layers on two sides of said submount wafer respectively, wherein the thickness of said first solderable layer is predetermined to compensate rough surface of said epitaxial layer;
   - pressingly bonding said reflective and Ohmic layers of said epitaxial wafer to said first solderable layer of said submount wafer to form a bonded semiconductor chip or devices wafer;
   - removing said substrate wafer from said bonded semiconductor chip or devices wafer so that said first confinement layer exposed;

- disposing patterned contact pads on said first confinement layer, wherein each of said patterned contact pads comprising at least one wire bonding pad;
- dicing said bonded semiconductor chip or device wafer into individual semiconductor chips or devices.

2. The wafer level flip chip package process of claim 1 wherein said substrate wafer is a sapphire wafer.
3. The wafer level flip chip package process of claim 2 wherein said sapphire wafer is removed by lapping and polishing process.
4. The wafer level flip chip package process of claim 1 wherein said substrate wafer is a Si wafer.
5. The wafer level flip chip package process of claim 4 wherein said Si wafer may be removed by plasma etching process.
6. The wafer level flip chip package process of claim 1 wherein said substrate wafer is a GaN wafer.
7. The wafer level flip chip package process of claim 6 wherein said GaN wafer may be removed by plasma etching process.
8. The wafer level flip chip package process of claim 1 wherein said reflective layer comprising materials selected from a group comprising Al, Au, and Ag.
9. The wafer level flip chip package process of claim 1 wherein said reflective layer is the distributed Bragg reflector.
10. The wafer level flip chip package process of claim 1 wherein the materials of said patterned contact layer are selected from a group comprising Al, Ni, Ti, and combinations thereon.

11. The wafer level flip chip package process of claim 1 wherein said submount wafer is selected from a group comprising SiC, Cu, Ag, and GaAs.
12. The wafer level flip chip package process of claim 1 wherein said first and second solderable layers is selected from a group comprising Au/Sn and Pb/Sn.
13. The wafer level flip chip package process of claim 1 further comprising a process step that a current spreading layer is sandwiched between said patterned contact pad and said first confinement layer.
14. A new flip chip assembly of semiconductor chips or devices comprising
    - an electrically and thermally conductive submount chip selected from materials of a group comprising SiC, Cu, Ag, and GaAs;
    - an epitaxial layer comprising a second confinement layer, an active layer, and a first confinement layer stacked on said submount chip;
    - reflective and Ohmic contact layers sandwiched between said epitaxial layer and said submount chip;
    - a patterned contact pad disposed on said first confinement layer wherein said patterned contact pad comprising at least one wire bonding pad.
15. The new flip chip assembly of semiconductor chips or devices of claim 14 wherein said reflective layer is a distributed Bragg reflector.
16. The new flip chip assembly of semiconductor chips or devices of claim 14 further comprising a current spreading layer sandwiched between said patterned contact pad and said first confinement layer.

17. The new flip chip assembly of semiconductor chips or devices of claim 14 wherein said patterned contact pad is a plus-ring-shaped contact pad with at least one wire bonding pad.

18. The new flip chip assembly of semiconductor chips or devices of claim 14 wherein said patterned contact pad is a grid-ring-shaped contact pad with at least one wire bonding pad.

19. The new flip chip assembly of semiconductor chips or devices of claim 14 wherein said patterned contact pad is a plus-multi-ring-shaped contact pad with at least one wire bonding pad.

20. The new flip chip assembly of semiconductor chips or devices of claim 14 wherein said patterned contact pad is a plus-multi-ring-partition-shaped contact pad with at least one wire bonding pad.

21. The new flip chip assembly of semiconductor chips or devices of claim 14 wherein said wire bonding pad being a strip-shaped wire bonding pad.

22. A new lamp for a flip chip assembly of semiconductor chips or devices comprising:

- a lead frame with reflective cup;
- a flip chip assembly disposed on said reflective cup and comprising an electrically and thermally conductive submount, an epitaxial layer disposed on said submount, a patterned contact pad disposed on said epitaxial layer;
- a hemisphere-shape material covering said flip chip assembly and having a radii R which is equal to or larger than R = nd where d is the half of the dimension of said flip chip assembly and n is the refractive index of said hemisphere-shape

material, and wherein said refractive index n is the same as that of said epitaxial layer.

23. The new lamp for a flip chip assembly of semiconductor chips or devices of claim 22 further comprising a neck portion for holding said hemisphere-shape material.

24. The new lamp for a flip chip assembly of semiconductor chips or devices of claim 22 further comprising a transparent cover.